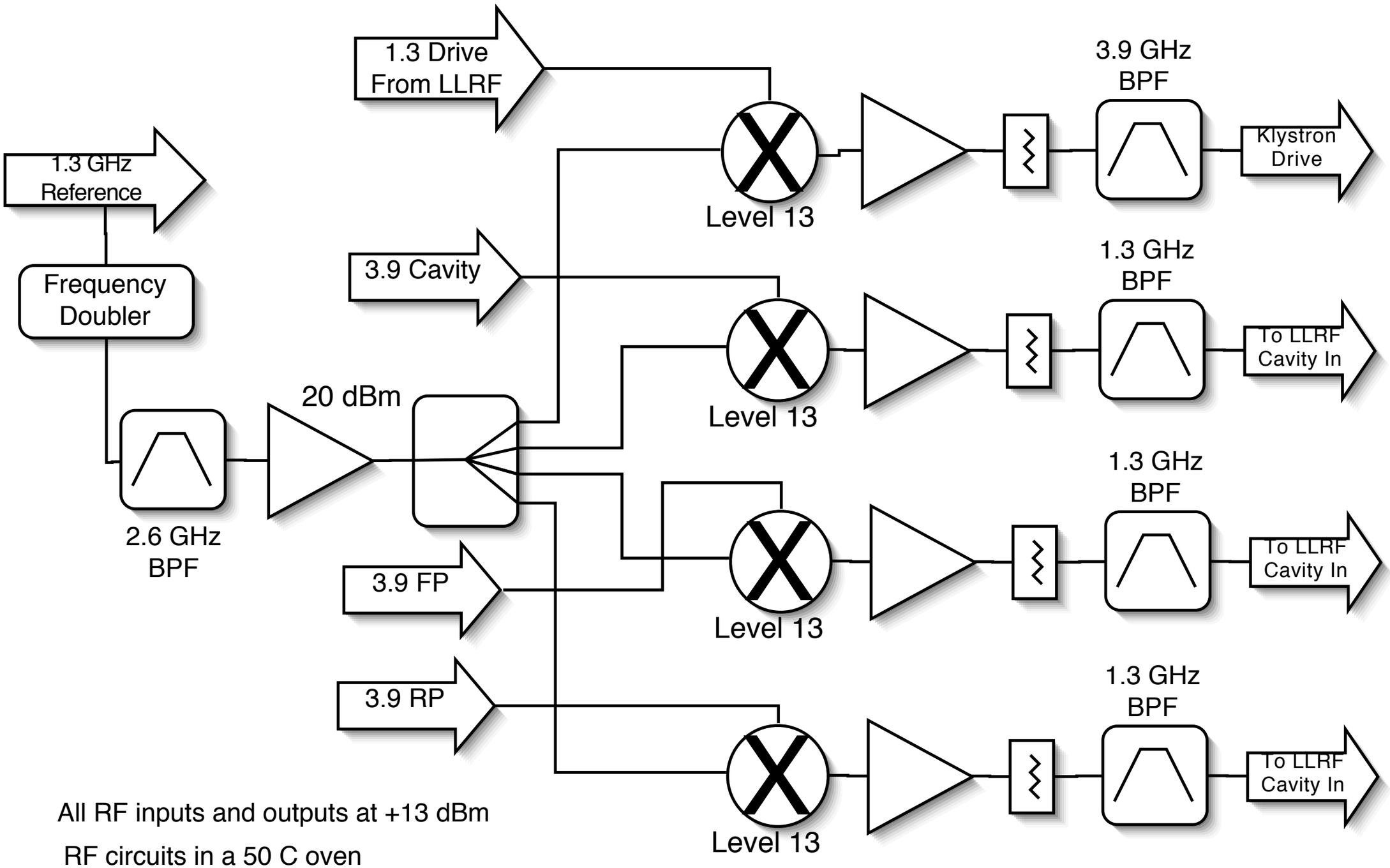
3.9 GHz SRF LLRF

Brian Chase AD, Ruben Carcagno TD, Gustavo Cancelo CD

1.3/3.9 GHz Up/Down Converter



All RF inputs and outputs at +13 dBm

RF circuits in a 50 C oven

Costs and Schedule

- Up/Down converter < ($10k x 4)
- Two to DESY, two for FNAL
- 1st prototype - 4 weeks
- Production - 14 weeks
- Engineering- Chase, Cullerton AD

LLRF Collaboration

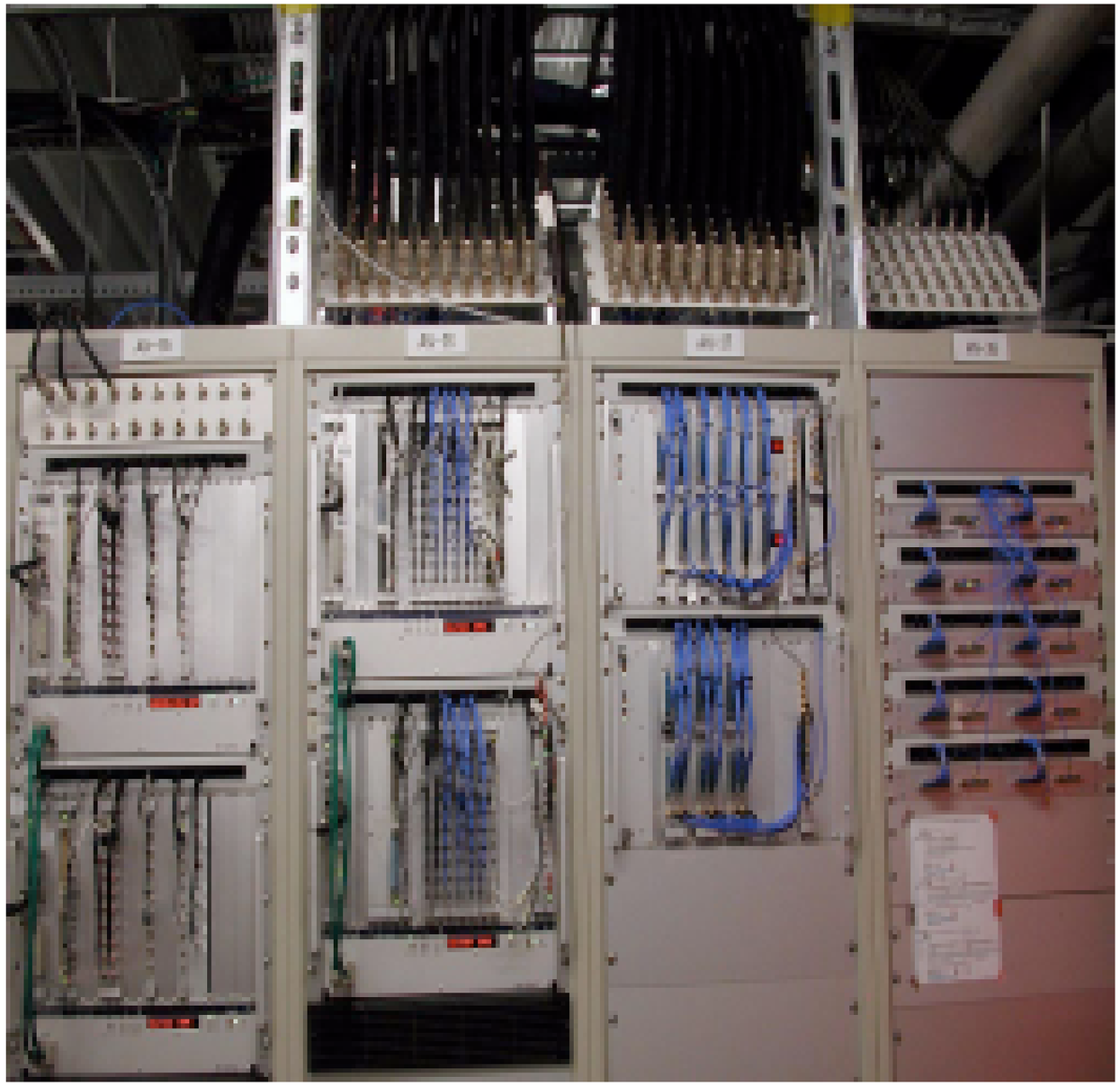
- Fermilab Accelerator, Technical, and Computing Divisions working as one LLRF team
- DESY, Penn State, and SNS
- HPTF will be a test bed for LLRF - tight regulation specs demand cross checking between systems
- HPTF has limited manpower and tight schedules
- Hardware designs are converging - why duplicate effort?
- Fermilab will add to hardware, firmware and software efforts that will transfer back to the other institutions
- Opportunity to compare and contrast systems

TTF LLRF

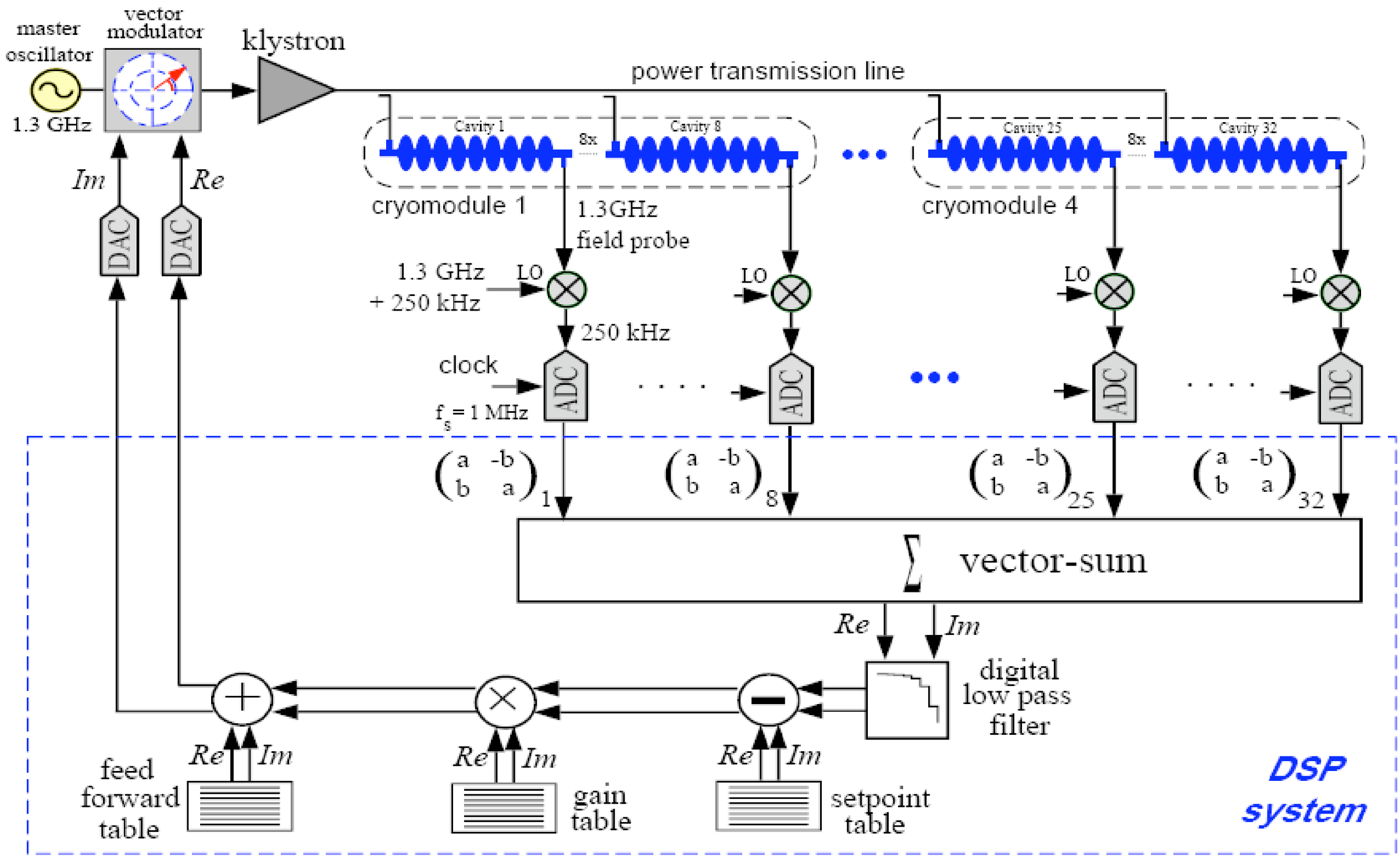
Digital Feedback Hardware

Gun and ACC1

ACC2, ACC3, ACC4 & ACC5

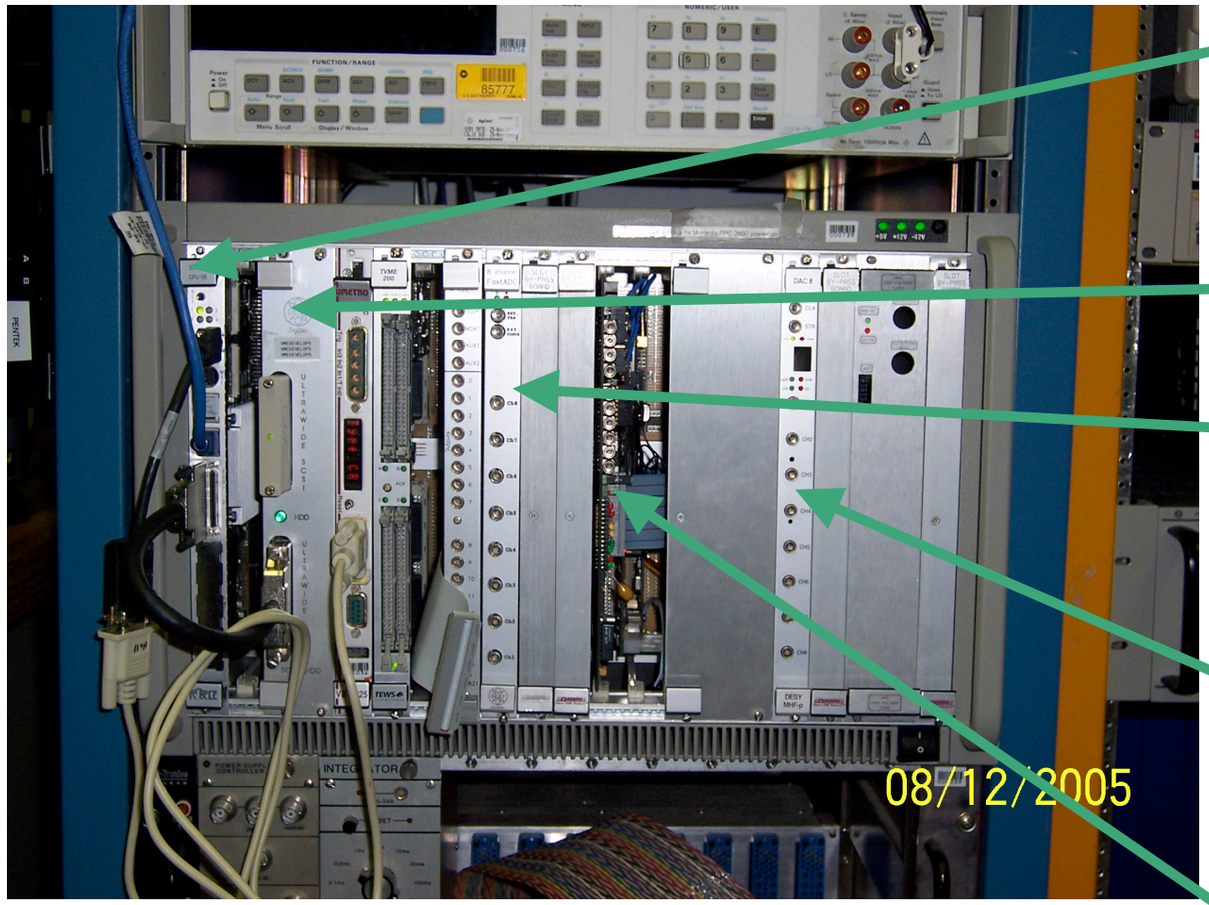


Digital Control at the TTF



First SMTF LLRF Crate (Simcon 2.1)

Simcon 2.1 has already been used at Fermilab to run the A0 Capture Cavity 1 several times



VME Modules:

-Sparc CPU-56 running DOOCS and Matlab

-Hard Disk

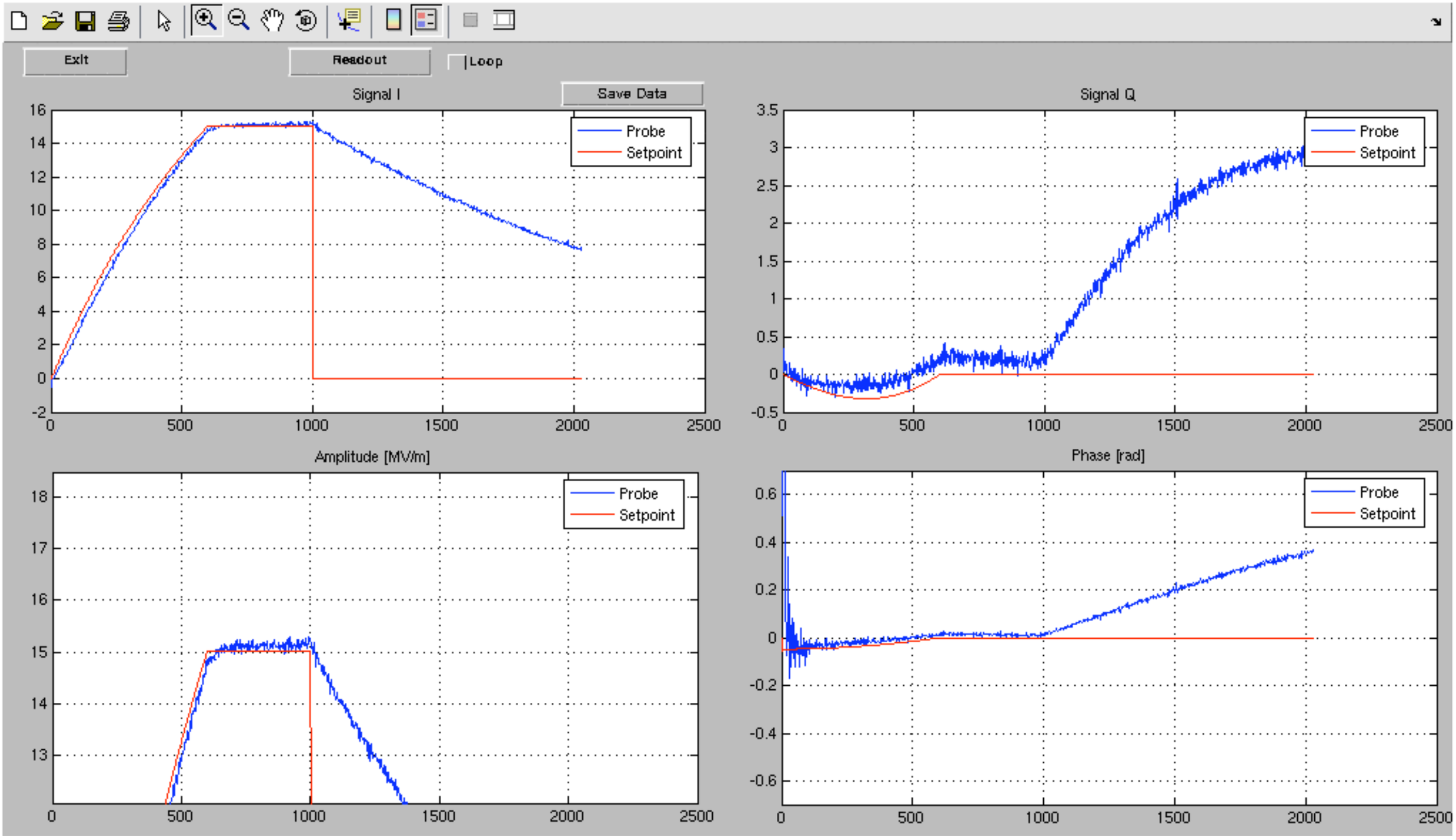
-8-Ch, 10 MHz fast digitizer (DESY design)

-8-Ch Function Generator board (DESY design)

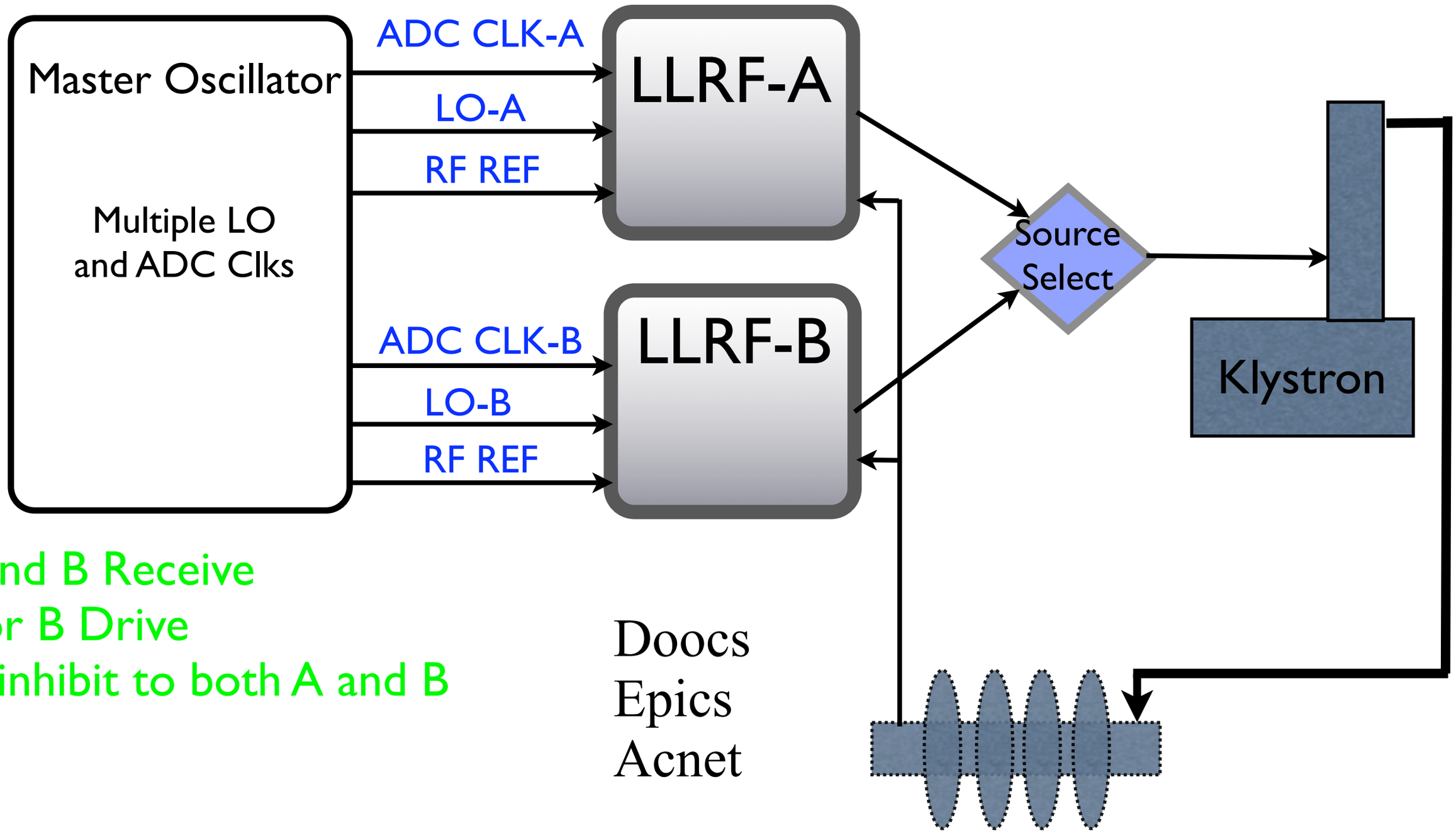
-Simcon 2.1 FPGA board (DESY design + commercial FPGA board)

Other Modules not shown: Master Oscillator, Timing board, Vector Modulator, Mixer, and fast RF switch

Simcon2.1 @A0 Gain = 40



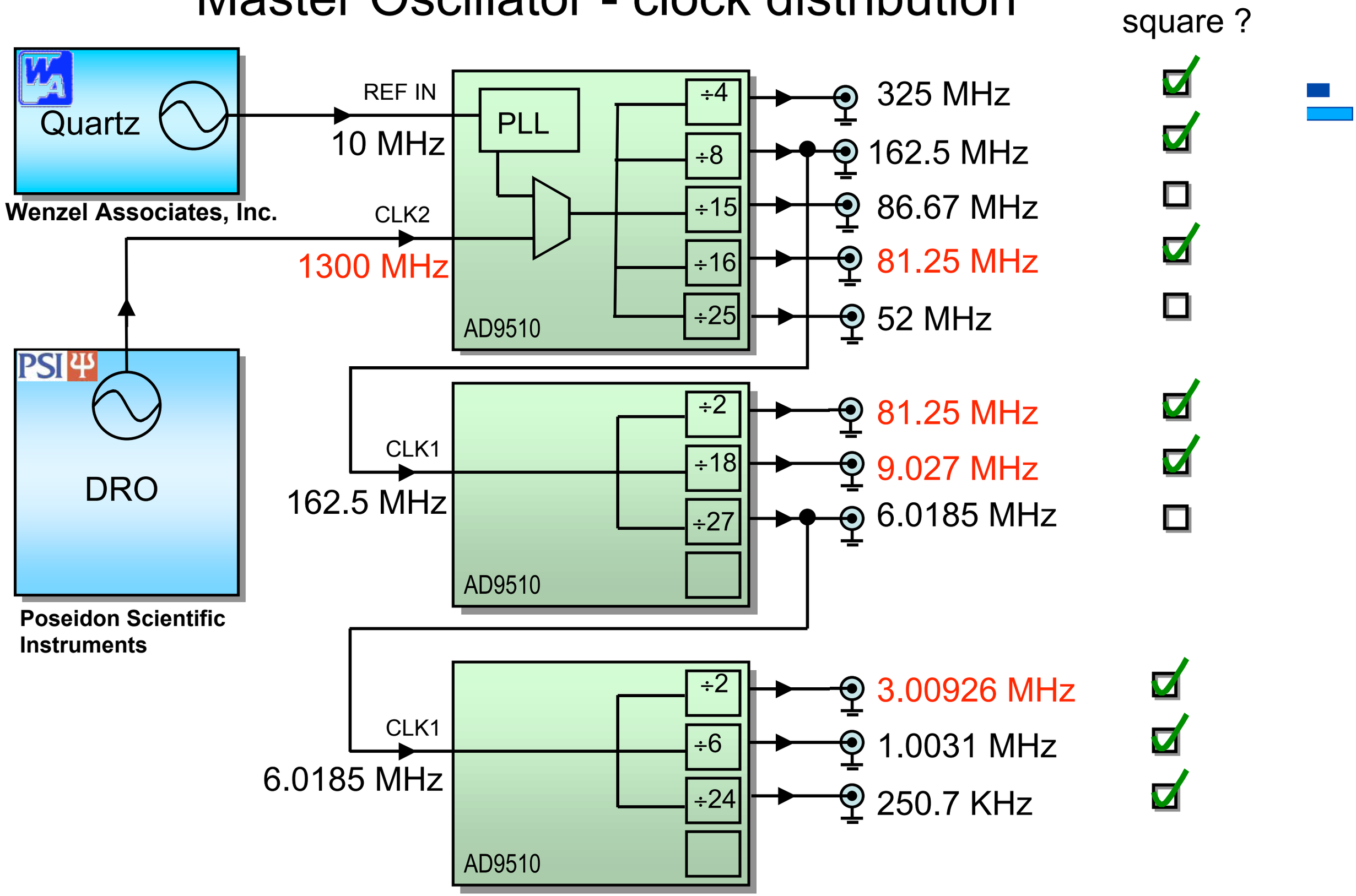
Dual LLRF Interface



A and B Receive
A or B Drive
RF inhibit to both A and B

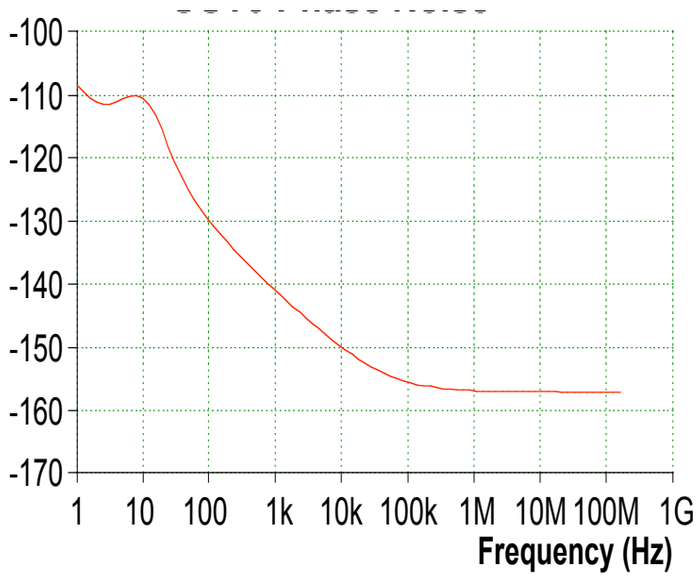
Doocs
Epics
Acnet

Master Oscillator - clock distribution

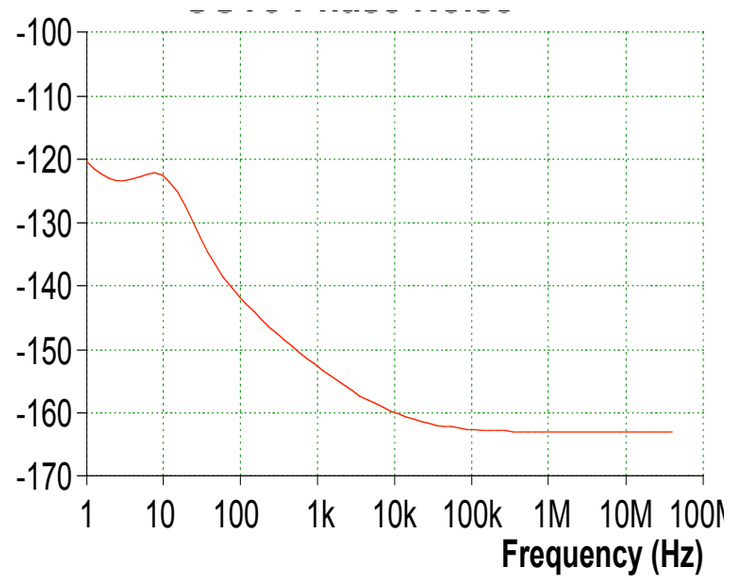


Master Oscillator - ADIsimCLK

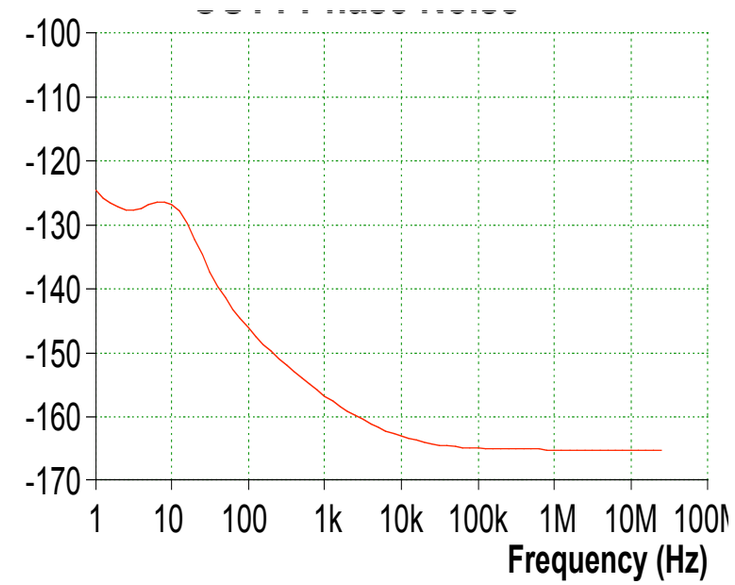
325.0 MHz



81.25 MHz



50.0 MHz



Phase noise

	325 MHz	86.67 MHz	**81.25 MHz**	**50 MHz**	9.028 MHz	3.010 MHz	1.003 MHz
100 Hz	**-130 dBc**	-142 dBc	**-142 dBc**	**-145 dBc**	-158 dBc	-151 dBc	-159 dBc
1 kHz	**-140 dBc**	-152 dBc	**-152 dBc**	**-156 dBc**	-167 dBc	-156 dBc	-161 dBc
10 kHz	**-150 dBc**	-160 dBc	**-160 dBc**	**-163 dBc**	-168 dBc	-157 dBc	-161 dBc
100 kHz	**-155 dBc**	-162 dBc	**-162 dBc**	**-165 dBc**	-169 dBc	-157 dBc	-162 dBc